IDM UID
CD899M
VERSION CREATED ON / VERSION / STATUS
10 Mar 2026 / 1.4 / Approved
EXTERNAL REFERENCE / VERSION

Interface Sheet-IS

IS-41-46-009 – Interface Sheet (IS) between V3PS Plant Interlock System of PBS41 and PBS46

IS-41-46-009

Approval Process			
	Name	*Action*	*Job Title / Affiliation*
Author	**Chiesa M.**	**10 Mar 2026:signed**	**Control Systems integration Enginee...**
Co-Authors	**Han J.** **Pince L.** **Van kessel R.**	**10 Mar 2026:signed** **11 Mar 2026:signed** **10 Mar 2026:signed**	**Instrumentation & Control Technicia...** **Nuclear System Integration Engineer** **Electrical Engineer**
Reviewers	**Fimbel C.** **Karkinsky D.** **Liu Y.** **Lopez-Villanueva R.** **Marqueta A.** **Shen H.** **Wilhelm B.**	**11 Mar 2026:recommended** **18 Mar 2026:recommended** **24 Mar 2026:recommended** **26 Mar 2026:recommended** **11 Mar 2026:recommended** **24 Mar 2026:recommended** **13 Mar 2026:recommended**	**Project Leader** **Interlock Systems Integration Engin...** **Interlock System Engineer** **Investment Protection Engineer** **Interlock Systems Responsible Offic...** **Project Leader** **Network & Infrastructure Engineer**
Approver	**Vanpoperynghe Y.**	**03 Apr 2026:approved**	**Section Leader**
Information Protection Level: Non-Public - Unclassified *RO: Tsedri Thibault*			
Read Access	**LG: DA RO to sign off ICDs, GG: AIF- CEA SSA Liaison Committee Members &experts, LG: F4E-Architect/Engineering company, GG: MAC Members and Experts, GG: STAC Members & Experts, GG: CEA Decommissioning Experts, LG: CEA view, GG: DA Heads, Co-ordinators and Management, AD: ITER, AD: External Collabor...**		

#drn#

Change Log			
IS-41-46-009 – Interface Sheet (IS) between V3PS Plant Interlock System of PBS41 and PBS46 (CD899M)			
Version	***Latest Status***	***Issue Date***	***Description of Change***
v0.0	In Work	11 Oct 2024	
v1.0	In Work	12 Feb 2026	First Version
v1.1	Revision Required	13 Feb 2026	Addressed comments from co-authors - see comments replies and 1.1 version with change bars in version 1.0
v1.2	In Work	09 Mar 2026	Updated according comments provided and results of f2f discussion from March 4, 2026 and follow-up emails as documented in V1.1 Added Han Jin as co-author and changed reviewers list.
v1.3	In Work	10 Mar 2026	Updated according comments provided and results of f2f discussion from March 4, 2026 and follow-up emails as documented in V1.1. Added Han Jin as co-author and changed reviewers list. Updated according to comments for IS-46-XX template.
v1.4	Approved	10 Mar 2026	corrected typo

Table of Contents

1 Purpose

This document IS-41-46-009 – Interface Sheet (IS) between V3PS Plant Interlock System of PBS41 and PBS46 (CD899M) defines the interface data and requirements which will be used for the design of both PBS 41.V3 and PBS 46.

2 Scope

The scope of this document is to define the interface points of this IS-41-46-009, which is propagated in the concerned ICD between the Coil Power Supply & Distribution (PBS-41) and the Central Interlock System (PBS 46) [AD1].

This document will:

- Identify the physical boundaries between PBS 41 VS3-PS system (41.V3) and PBS 46.
- Identify the functional interfaces between PBS 41 VS3-PS system (41.V3) PIS and PBS 46 CIS. The type of the functional interfaces, the communication protocols or tools.
- Identify the roles and responsibilities of both PBSs.

3 Definitions

For a complete list of ITER abbreviations see ITER Abbreviations 2MU6W5

CIS	Central Interlock System
CIN-P	Central Interlock Network for Process
CNP	Central I&C network panel
CP	Communication Processor
CPU	Central Processing Unit
DT-1	Deuterium-Tritium phase 1
DT-2	Deuterium-Tritium phase 2
F-LIC	Fast Local Interlock Controller
FO	Fiber optics (cable)
F-PIC	Fast Plant Interlock Controller
HIOC	High Integrity Operator Commands
ICD	Interface Control Document
IP	Interface Point
IP address	Internet Protocol address
IPF	Investment Protection Function
IS	Interface Sheet
LIC	(Slow) Local Interlock Controller
OSI	Open Systems Interconnection
MC	Manchester Code
PBS	Plant Breakdown Structure
PIC	Slow Plant Interlock Controller
PIS	Plant Interlock System
SRO	Start of Research Operations

tbc	to be confirmed
tbd	to be defined
VLAN	Virtual Local Area Network
V3 / VS3	Vertical Stabilization System 3
VS3-PS	Vertical Stabilization System 3- Power Supply

4 References

4.1 Applicable Documents

Ref	Document Titles	IDM UID	Version
[AD1]	ICD between PBS 41 and PBS 46	2M58GX	4.0
[AD2]	SRD-46 (Central Interlock System) from DOORS	2EVTP5	5.2
[AD3]	SRD-41 (Coil Power Supply and Distribution) from DOORS	28B6XQ	6.0
[AD4]	Plant Control Design Handbook	27LH2V	7.1
[AD5]	Staged Approach Configuration - PBS Level 3	SNE6G8	4.1
[AD6]	ITER_4601IN_CBD_002: CIN Plant Systems I&C Connections	U8L6T3	tbd[1]
[AD7]	PBS 41 (Except PP) - Coordinates of equipment (except EE in the TKC)	CRM2SE	1.9

4.2 Reference Documents

Ref	Document Titles	IDM UID	Version
[RD1]	Central Interlock System (PBS-46) - Design Description Document (DDD)	QCH3GJ	2.6
[RD2]	Guidelines for the Design of the Plant Interlock System (PIS)	3PZ2D2	5.0
[RD3]	Guidelines for PIS configuration and integration	7LELG4	4.0
[RD4]	PIS Operation and Maintenance	7L9QXR	3.0
[RD5]	HIOC: Software System Design (SDS)	WVEWGU	2.0
[RD6]	IDS-41-46-009 Interface Data Sheet (IDS) between VS3-PS of PBS41 and CIS of PBS46	tbd	x.x
[RD7]	Conceptual I&C Diagram for VS3 Power Supply System	EEKZGH	2.0
[RD8]	MPP.2.14.01 - MPP Record of Decision - IVC Power Supply	9E36DN	1.1

[1] This document shall be updated with the content of this IS after FDR/CCR of VS3-PS

[RD9]	MPP RoD - CPSS (Coil Power Supply System) - Fast interfaces PF/CS/VS1/VS3 <-> CIS for signalling Loss of Circuit Control E-MVS-FPIC_VS3_CONTROL_LOST-HI-E11244	CC978F	1.0
[RD10]	E-MVS-VS3-STOP_CODE-E11xxx	FPWLRZ	tbd
[RD11]	A-MVS-FPIC_VS3_POWER_SWITCH_OFF-E11xxx	tbd	x.x
[RD12]	A-MVS-FPIC_VS3_OUTPUT_OFF-E11xxx	tbd	x.x
[RD13]	MPP.2.02 GDC - MPP Record of Decisions A-MVS-VS3_POWER_PERMIT-E11xxx	5DXL5E	2.1

5 Description of interfaces and responsibilities

The main purpose of this IS is to define the physical and functional interfaces between PBS 46 and PBS 41.V3 for the implementation of the following Investment Protection Functions (IPF) per [RD8] and [RD9]:

The implementation of Central IPF's (CIS scope) relies on critical data (events and actions) exchanged with the plant systems (PBS PIS):

- Events: interlock events detection by PIS and communicated to CIS (PIS→CIS), the list of events received from the PIS are detailed in Chapter 5.2.1
  - E-MVS-VS3-STOP_CODE-LS_E11xxx [RD10]
  - E-MVS-FPIC_VS3_CONTROL_LOST-HI-E11244[RD9]
- Actions: coordination of PBS interlock actions by CIS (CIS→PIS), the list of actions commanded to the PIS are detailed in Chapter 5.2.2
  - A-MVS-FPIC_VS3_POWER_SWITCH_OFF-E11xxx [RD11]
  - A-MVS-FPIC_VS3_OUTPUT_OFF-E11xxx [RD12]
  - A-MVS-VS3_POWER_PERMIT-E11xxx [RD13]

List of interface points with their applicability as per the staged approach

The Table 5-1 below lists all the interface points, and for each of them identifies the PBS nodes and the phase of the staged approach [AD5] at which it is applicable.

IP number	PBS 46		PBS 41.V3		SRO	DT-1	DT-2
	System	PA	System	PA			
IP 1 - Physical interfaces							
IP 1.1 - Network architecture interface between PBS 41 VS3-PS PIS and CIS	46.01.IN	4.5.P1.IO	41.V3	na	X	X	X
IP 1.2 - Point-to-Point fibre optic interface between PBS 41 VS3-PS F-PIS and CIS	46.01.IN	4.5.P1.IO	41.V3	na	X	X	X
IP 2 - Functional interfaces							
IP 2.1: Events from PBS 41 VS3-PS PIS to CIS	46.01.CD	4.5.P1.IO	41.V3	na	X	X	X
IP 2.2: Actions from CIS to PBS 41 VS3-PS PIS	46.01.CD	4.5.P1.IO	41.V3	na	X	X	X

IP 2.3: Functional interface implementation	46.01.CD 46.02.SD	4.5.P1.IO	41.V3	na	X	X	X
IP 2.3.1 Critical automatic data for PBS 41 VS3-PS slow PIC	46.01.CD	4.5.P1.IO	41.V3	na	X	X	X
IP 2.3.2 Critical manual data for PBS 41 VS3-PS slow PIC	46.02.SD	4.5.P1.IO	41.V3	na	X	X	X
IP 2.3.3 Critical automatic data for PBS 41 VS3-PS F-PIC	46.01.CD	4.5.P1.IO	41.V3	na	X	X	X
IP 2.3.4 Critical manual data for PBS 41 VS3-PS F-PIC	46.02.SD	4.5.P1.IO	41.V3	na	X	X	X
IP 2.3.5: PIS supervision data for slow PIC	46.02.SD	4.5.P1.IO	41.V3	na	X	X	X
IP 2.3.6: Archiving data for Slow PIC	46.02.SD	4.5.P1.IO	41.V3	na	X	X	X
IP 2.3.7: PIS supervision data for F-PIC	46.02.SD	4.5.P1.IO	41.V3	na	X	X	X
IP 2.3.8: Archiving data for F-PIC	46.02.SD	4.5.P1.IO	41.V3	na	X	X	X

Table 5-1: Interface points between PBS 46 and PBS 41 VS3-PS

5.1 IP 1: Physical interfaces

This section describes the physical interface between both systems, i.e. where components of one system physically meet the components of the other.

The physical interfaces identified are:

- Network architecture interface between PBS41 VS3-PS PIS (PLC's and Fast-Host servers) and CIS
- Point-to-Point fibre optic links for the fast architecture (cRIO to cRIO), between VS3-PS fast PIS and CIS

5.1.1 IP 1.1: Network architecture interface between PBS 41 VS3-PS PIS and CIS

5.1.1.1 Network architecture interface

This section describes the physical interface between PBS 41 VS3-PS PIS and CIS through the network.

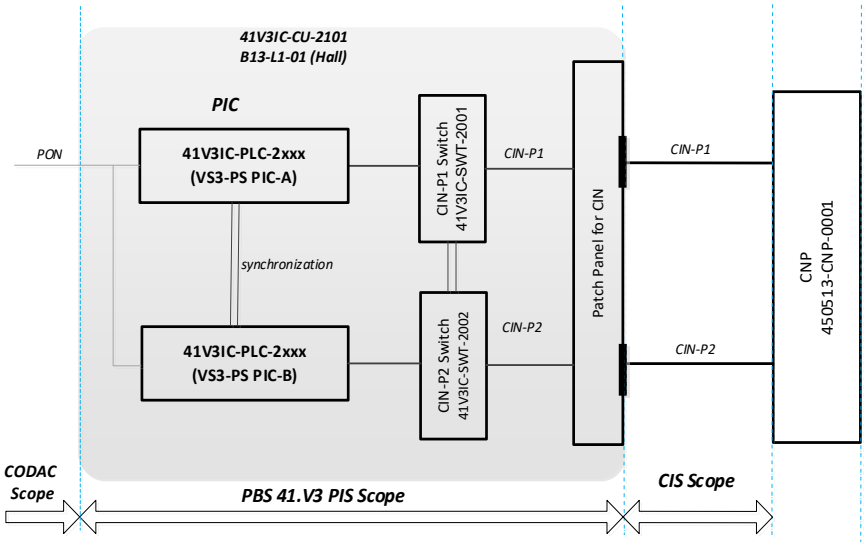

Figure 5-1: Slow architecture interfaces between CIS and PBS 41 VS3-PS Slow PIS

Note: The connection of the Plant Interlock Controllers with PON and TCN is out of the scope of this document. Please refer to the IS between PBS 41 VS3-PS and PBS 45.

PBS 41 VS3-PS plant interlock system interfaces to CIS via CIN-P network infrastructure in order to send or receive critical data to/from CIS for central interlock function and sends non-critical data to CIS for supervision. CIS provides CIN-P redundant connections by routing two FO patch cables, CIN-P1 and CIN-P2 (single mode, 9/125 µm, LC interface), to cubicle **41V3IC-CU-2101**. CIN-P1 and CIN-P2 (in the scope of CIS) are respectively connected to PBS 41 VS3-PS CIN-P switches 41V3IC-SWT-2001 and 41V3IC-SWT-2002 which in turn propagate the network to the fast / slow interlock controllers. The network interface architecture between PBS 41 VS3-PS and CIS is shown in figure 5-1 (connection to fast-host is captured in figure 5-2).

For the coordinates of **41V3IC-CU-2101** in building 13, pls. refer to [AD7].

[41.46-009i1-R] *The PBS 41 VS3-PS PIS shall have 2 CIN-P switches for redundant connection to PBS 46 CIN-P network.*

[41.46-009i2-R] *The uplink ports of the CIN-P switches shall be optical Gigabit Ethernet ports.*

[41.46-009i3-R] *The uplink ports of the CIN-P switches shall be equipped with LC-type connectors.*

[41.46-009i4-R] *The CIN-P switches shall operate at a wavelength of 1310 nm, suitable for single-mode fiber transmission.*

[41.46-009i5-R] *The OSI Layer Functionality of CIN-P switches shall operate at Layer 2 (Data Link Layer) of the OSI model, enabling MAC address-based switching and frame forwarding.*

[41.46-009i6-R] *The VLAN Support of CIN-P switches shall support IEEE 802.1Q VLAN tagging, capable of managing multiple VLANs and supporting inter-VLAN routing if required.*

[41.46-009i7-R] *The Redundancy and Link Aggregation of CIN-P switches shall support RSTP (Rapid Spanning Tree Protocol) – IEEE 802.1w – for fast convergence and loop prevention.*

[41.46-009i8-R] *The Redundancy and Link Aggregation of CIN-P switches shall support LACP (Link Aggregation Control Protocol) – IEEE 802.3ad – for dynamic link aggregation and redundancy.*

[41.46-009i9-R] *For the PBS 41 VS3-PS PIS cubicle connection, PBS 46 shall provide two CIN redundant SMF patch cables to the PBS 41 VS3-PS CIN Patch Panel inside the PBS 41 VS3-PS PIS cubicle. The interface point is on the PBS 41 VS3-PS CIN Patch Panel.*

[41.46-009i10-R] *The cabling of CIN within an I&C cubicle or between I&C cubicles of PBS 41 VS3-PS shall be in the scope of PBS 41 VS3-PS.*

5.1.1.2 Network IP address allocation

CIS assigns and manages following PIS IP address:

- The CIN IP addresses for the Plant Interlock Controller Figure 5-1.
- The CIN IP addresses for the network switches indicated in Figure 5-1.
- The CIN IP addresses for fast controllers host PCs indicated in Figure 5-2.

[41.46-009i11-R] *PBS 46 shall allocate an IP address to each of the component of PBS 41 VS3-PS PIS connected to CIN-P.*

The IP addresses are listed in Table 7-2.

5.1.2 IP 1.2: Point-to-Point fibre optic interface between PBS 41 VS3-PS F-PIS and CIS

This section describes the physical interface between PBS 41 VS3-PS fast controller PIS (F-PIS) and CIS through point-to-point fibre optic.

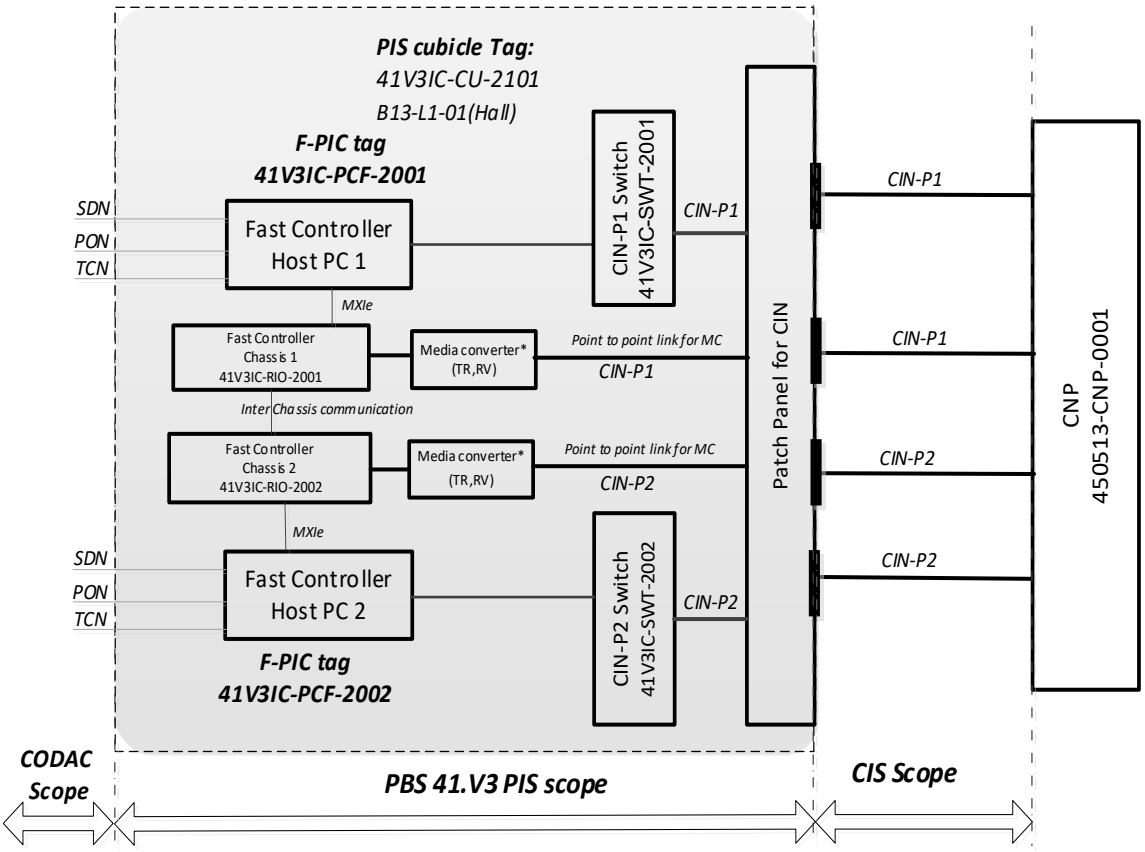

Figure 5-2 Fast architecture interface between PBS 41 VS3-PS F-PIS and CIS (see remark *)

Note: The connection of the Plant Interlock Controllers with PON/TCN/SDN is out of the scope of this document. Please refer to the IS between PBS 41 VS3-PS and PBS 45.

The CIS provides redundant connections by routing two FO patch cables to cubicle 41V3IC-CU-2101.

PBS 41 VS3-PS fast plant interlock system interfaces to CIS via point-to-point links in order to send or receive critical data to/from CIS for central interlock function, each point-to-point link uses a fibre of the CIN-P backbone cable. The interface point is on the CIN patch panel installed in the PIS cubicle. The fast controller chassis are connected to the CIN patch panel via media converters.

Each of the host PC interface to CIN-P via a CIN-P switch. The CIN-P switch can be dedicated for the F-PIS, or shared with the VS3-PS slow interlock controllers.

[41.46-009i12-R] *The PBS 41 VS3-PS F-PIS cubicle shall have two media converters for redundant connection to PBS 46 CIN-P network (1oo2 logic). Remark *:The media converters are both way as the communication is both directions. In case the 1oo2 logic of the signalling does not provide the required availability, a 2oo3 logic shall be selected, which would require a 3rd media converter and a 3rd point-to-point connection. Alternative to the 2oo3 would be an additional "ENABLE" which requires 2 additional point-to-point connections with 2 media converters.*

[41.46-009i13-R] *PBS 41 VS3-PS F-PIS design shall respect the PBS 46 electrical characteristic for the physical interface.*

5.2 IP 2: Functional interfaces- Central Interlock Events/Actions exchanged

Central interlock events are the plant system state or combination of states that, managed by the corresponding PIS, are propagated to CIS which, following the central-IPF logic, will further trigger the required action or group of actions.

Central interlock actions are measures or sequence of measures carried out by the CIS to mitigate the risks following an interlock event. These protection actions are managed by the PIS, following the command of the CIS as a result of the execution of a central-IPF.

Investment Protection related actions are assigned as protection layers but implemented by conventional control systems. As conventional control is not qualified to implement 3IL rated investment protection functions, these are backed up via escalation by another protection function implemented in the CIS-PIS chain [RD1].

5.2.1 IP 2.1: Events from PBS 41 VS3-PS PIS to CIS

The list of events from PBS 41 VS3-PS PIS to CIS are below:

- E-MVS-VS3-STOP_CODE-LS_E11xxx – Upcoming shutdown

  VS3-PS send the stop-code event to CIS indicating the upcoming shutdown due to temperature, lack of cooling water flow or other reasons. The details of the event are available in E-MVS-VS3-STOP_CODE-LS_E11xxx [RD10].This communication is critical and realtime[2] and described in Chapter 5.3.1.

  Note: it is still to be defined if the stop code will be send via Slow PIS interface or Fast PIS interface.

- E-MVS-FPIC_VS3_CONTROL_LOST-HI-E11244 - VS3-PS loss of circuits control

[2] If there is time boundary for the Event, it is realtime. Otherwise it is non-realtime.

VS3-PS send the loss of circuit control, i.e. loss of vertical stabilization to CIS. The details of the event are available in E- MVS-FPIC_VS3_CONTROL_LOST-HI-E11244 [RD9]. This communication is critical and **realtime** and described in Chapter 5.3.3.

5.2.2 IP 2.2: Actions from CIS to PBS 41 VS3-PS PIS

The list of actions from CIS to PBS 41 VS3-PS PIS are below:

- A-MVS-FPIC_VS3_POWER_SWITCH_OFF-E11xxx – VS3-PS power switch off. CIS requests the immediate switch off. The details of the action are available in A-MVS-FPIC_VS3_POWER_SWITCH_OFF-E11xxx [RD11]. This communication is critical and **realtime** and described in Chapter 5.3.1
- A-MVS-FPIC_VS3_OUTPUT_OFF-E11xxx – VS3-PS output off. CIS requests the immediate output off. The details of the action are available in A-MVS-FPIC_VS3_OUTPUT_OFF-E11xxx [RD12]. This communication is critical and **realtime** and described in Chapter 5.3.15.3.1
- A-MVS-VS3_POWER_PERMIT-E11xxx – VS3-PS power permit on

  CIS permits VS3-PS to start. The details of the action are available in A-MVS-VS3_POWER_PERMIT-E11xxx [RD13]. This communication is critical and non-realtime and described in Chapter 5.3.1.

5.3 IP 2.3: Functional interfaces implementation

There are four categories of functional interfaces between the PBS 41 VS3-PS plant interlock controllers (both for slow and fast controllers) and the CIS corresponding modules:

- Critical automatic data
- Critical manual data
- PIS supervision data
- Archiving data

The functional interface data are documented and managed through the IDS (Interface Data Sheet) (Chapter 7.2).

Data exchanged between CIS modules and PIS which directly involves the execution or configuration of central interlock functions (events, actions) are considered critical (interlock) data. Critical data generated automatically (i.e. automatic execution of an IPF) are called critical automatic data. Critical data managed by the operator from the CIS desk, for the purpose of IPF configuration (masking, thresholds, etc) are called critical manual data. Certain protection functions could eventually also be manually triggered by the CIS operator.

Supervision data is data that is sent from PIS to CIS for the monitoring of all critical status (event, action, etc.) of the protection functions and critical PIS health monitoring data and PIS diagnostic data. Such data is considered non-critical.

Archiving data is the data sent from PIS to CIS for all the critical events and actions of PIS logged together with their own time stamp, which are assigned directly by the triggering PIS. Such data is also considered non-critical.

5.3.1 IP 2.3.1 Critical automatic data for PBS 41 VS3-PS slow

[41.46-009i14-R] *PBS 41 VS3-PS shall allow CIS to manage the process to merge the different slow PIC PLC S7 projects interfacing CIS into one S7 "Multiproject".*

[41.46-009i15-R] *The critical automatic data between PBS 41 VS3-PS slow PIC and CIS shall be exchanged based on SIEMENS S7 fault tolerant connections with a safety message frame (F_SEND/F_RCV) between the F-CPU (communication via CIN-P).*
Critical automatic data for slow PIC are the data exchanged between CIS and slow PIC necessary for the management of events and actions described in Chapter 5.2.1 and 5.2.2. These data include (but not limited to): PIS modules, variable name in PIS modules, variable address in PIS modules with connection details, variable descriptions, CIS modules, variable address in CIS modules with connection details, communication directions, communication protocol, etc. The details are documented in IDS (Chapter 7.2).

5.3.2 IP 2.3.2 Critical manual data for PBS 41 VS3-PS slow PIC

Critical manual data for slow PIC are the data exchanged between CIS and slow PIC for the implementation of following manual commands, sent from the CIS desk to the slow PIC:

- Masking an interlock event – *Override command to mask the potential occurrence of an interlock event from PIC to CIS*
- Enabling/disabling an interlock function – *Override command to enable/disable an interlock function*
- Forcing an interlock action – *Override command to force an interlock action*
- Interlock Configuration Data (Threshold Selection etc.)

More specifically, the slow PIC exchanges critical manual data with the Supervisor Module of CIS. To ensure that a critical manual command is applied to the correct PLC in the PIS and to the right function, a specifically developed HIOC application protocol (over Standard S7 communication) is used in [RD5].

[41.46-009i16-R] *PBS 46 shall send the critical manual data from CIS Supervisor Module to PBS 41 VS3-PS slow PIS.*

[41.46-009i17-R] *HIOC protocol (over Standard S7 communication) shall be implemented both in the CIS Supervisor Module and PBS 41 VS3-PS slow PIS.*

[41.46-009i18-R] *The HIOC library delivered by PBS 46 shall be deployed/used in the PBS 41 VS3-PS slow PIC.*

The critical manual data shall include the override for events and actions for slow PIC in previous Chapter 5.3.1, including (but not limited to): Object name in Supervisor Module, Object description, PIS module, Chart name in PIS modules, override commands, controller ID, function ID, command ID, Confirmation ID, Communication protocol, PBS number (PP), (controller number(XXXX), command code(CC), etc.

5.3.3 IP 2.3.3 Critical automatic data for PBS 41 VS3-PS F-PIC

[41.46-009i19-R] *The critical automatic data PBS 41 VS3-PS F-PIC and PBS 46 fast controllers shall be performed using Manchester Code (MC[3]) communication over redundant[4] optical links.*

Critical automatic data for F-PIC are the data exchanged between CIS and PBS 41 VS3-PS F-PIC necessary for the management of events and actions described in previous Chapter 5.2.1 and 5.2.2, including (but not limited to):

- MC input Events table with detailed packet structure (CRC, Bytes list, Counter, etc.)
- MC output Actions table with detailed packet structure (CRC, Bytes list, Counter, etc.).

[3] tbc – the usage of MC instead of optical signals is to be confirmed.
[4] tbc – usage of redundant (1oo2) point-to-point signaling lines could be replaced by 2oo3 point-to-point signaling lines or an alternative confirmation logic (e.g. additional ENABLE signal lines)

5.3.4 IP 2.3.4 Critical manual data for PBS 41 VS3-PS F-PIC

Critical manual data for F-PIC are the data exchanged between CIS and PBS 41 VS3-PS F-PIC for the implementation of following manual commands, sent from the CIS desk to the F-PIC:

- Masking an interlock event – *Override command to mask the potential occurrence of an interlock event from PIC to CIS*
- Enabling/disabling an interlock function – *Override command to enable/disable an interlock function*
- Forcing an interlock action – *Override command to force an interlock action*
- Interlock Configuration Data (Threshold Selection etc.)

The operations for the override shall be settable through the HIOC protocol which is implemented both in CIS Supervisor Module and F-PIC, driving correctly the corresponding flags.

[41.46-009i20-R] *Each host PC of the PBS 41 VS3-PS F-PIC shall be connected to CIN patch panels via CIN-P switches using TCP/IP communication protocol.*

[41.46-009i21-R] *PBS 46 shall send the critical manual data from CIS Supervisor Module to PBS 41 VS3-PS F-PIC fast PIS.*

[41.46-009i22-R] *HIOC protocol shall be implemented both in the CIS Supervisor Module and PBS 41 VS3-PS fast PIS.*

5.3.5 IP 2.3.5: PIS supervision data for slow PIC

The following supervision data of slow plant interlock controller are monitored at CIS desk:

- Slow plant interlock controller hardware health status: CPU, CP, I/O module and etc.
- The discrepancy status of voters: voter for digital input, voter for analogue input and voter for threshold.
- Ready to Reset from PIS
- The health state of Event and Action: OK, degraded, fault
- The PIS health monitoring data
- The action execution feedback data
- The raw status of following data:
  - The event which can be masked and the masking status;
  - The function which can be disabled and the disabling status;
  - The action which can be forced and the forcing status.

[41.46-009i23-R] *PBS 41 VS3-PS shall send PIS supervision data from PBS 41 VS3-PS slow PIS to PBS 46 Supervisor Module via standard S7 protocol.*

5.3.6 IP 2.3.6: Archiving data for slow PIC

Following the occurrence of events/actions, some information are to be transferred from PIC to CIS for archiving purpose. The archiving data of an event/action includes:

- The status of plant interlock system events/actions which are involved with the central interlock functions.
- Whether the local interlock function is activated.
- Whether the local interlock function is reset.

The archiving data is sent from the plant interlock controller to the CIS supervisor module. All events generated are logged together with their own time stamp, which are managed directly by the triggering controller device.

The connections between the slow plant interlock controller and the CIS supervisor modules are based on S7-TSPP (Time Stamp Pushed Protocol) which enable spontaneous transmission of data and the generation of time stamps in the plant interlock controller, in this case the plant interlock controller prepares a defined data buffer with the data to be transferred and send this data using a BSEND PLC function call.

[41.46-009i24-R] *PBS 41 VS3-PS shall send PIS archiving data from PBS 41 VS3-PS slow PIS to PBS 46 Supervisor Module via S7 TSPP protocol which enable spontaneous transmission of data and the generation of time stamps in the plant interlock controller.*

[41.46-009i25-R] *The TSPP library delivered by PBS 46 shall be used in the PBS 41 VS3-PS slow PIC.*

5.3.7 IP 2.3.7: PIS supervision data for F-PIC

The following data of fast plant interlock controller are monitored at CIS desk:

- Fast plant interlock controller hardware health status, chassis status, synchronization status.
- The diagnostic data.
- The raw status of the following data: voter inputs, voter outputs, reset status, ready to reset, latch, OVRS, CRT and CRTO values of each overridable interlock event/action.
- Ready to Reset from PIS
- The health state of Event and Action: OK, degraded, fault
- The PIS health monitoring data
- The action execution feedback data

The supervision data are sent from F-PIC to CIS Supervisor Module through OPC UA communication protocol.

[41.46-009i26-R] *The OPC UA server shall be provided in PBS 41 VS3-PS F-PIC host to interface with OPC UA client in CIS Supervisor Module.*

5.3.8 IP 2.3.8 Archiving data for F-PIC

Following the occurrence of events/actions, some data shall be transferred from F-PIC to CIS for archiving purposes. The event/action archiving data include:

- The fast plant interlock system status of the events/actions which are involved with the central interlock functions.
- Whether the local interlock function is activated.
- Whether the local interlock function is reset.
- The timestamp OVRS bit changed state.
- The timestamp CRTO bit changed state.
- The timestamp CRT bit changed state.

The archiving data are sent from F-PIC to CIS Supervisor Module through OPC UA communication protocol. The OPC UA server runs in F-PIC's host PC, while the CIS Supervisor Module acts as OPC UA client. The concept of supervision on PIS is explained in 5.2.1 of [RD3]. It is advised that the HIOC FPGA library delivered by PBS 46 is incorporated in the F-PIC design**.**

[41.46-009i27-R] *In order to handle supervision data, archiving data and critical manual data between F-PIC's Host PC and CIS Supervisor Module, OPC UA communication link shall be deployed and used.*

5.4 Scope and Responsibilities

5.4.1 Network and optic fibre communications

- PBS 46 is responsible for providing and installing the patch cord cables (CIN-P cables) between the CNP and cubicle 41V3IC-CU-2101.
- PBS 41 VS3-PS is responsible for providing PBS 46 with the CIN-P switches location for the proper connection of PBS 46 CIN-P cables.
- PBS 41 VS3-PS is responsible to connect the CIN-P networks between PBS 41 VS3-PS plant interlock controllers (fast and slow) and CIN-P switches.

5.4.2 OPC UA communication

- PBS 46 is responsible for OPC UA client configuration in the CIS Supervisor Module.
- PBS 41 VS3-PS is responsible for OPC UA server configuration in F-PIC host.

5.4.3 Functional integration

- PBS 46 shall provide support to PBS 41 VS3-PS for HIOC library deployment, implementation and configuration.
- PBS 46 provide support to PBS 41 VS3-PS for OPC UA server deployment and implementation in F-PIC host
- PBS 46 and PBS 41 VS3-PS must collaborate to produce the technical specifications for Central Interlock Events/Actions/Functions.
- PBS 46 and PBS 41 VS3-PS must collaborate to perform IPF verification and validation.

6 Requirements

6.1 Generic Requirements

The design requirements defined in Plant Control Design Handbook for interlock I&C specifications [AD4] shall be followed.

The interlock control systems shall be designed such that the architecture, hardware and software are homogeneously designed with the ITER project control system.

The physical and functional interfaces shall be designed to meet the IPF specifications in[RD8], [RD9], [RD10], [RD11], [RD12] and [RD11][RD13].

Following guidelines can be followed to help designing in consistency with requirements:

- Guidelines for the Design of the Plant Interlock System (PIS) [RD2]
- Guidelines for PIS configuration and integration [RD3].

6.2 Summary of Interface Requirements (IR)

IR identifier	IR	IR Responsible
[41.46-009i1-R]	The PBS 41 VS3-PS PIS shall have 2 CIN-P switches for redundant connection to PBS 46 CIN-P network	PBS 41 VS3-PS
[41.46-009i2-R]	The uplink ports of the CIN-P switches shall be optical Gigabit Ethernet ports	PBS 41 VS3-PS
[41.46-009i3-R]	The uplink ports of the CIN-P switches shall be equipped with LC-type connectors	PBS 41 VS3-PS
[41.46-009i4-R]	The CIN-P switches shall operate at a wavelength of 1310 nm, suitable for single-mode fiber transmission.	PBS 41 VS3-PS
[41.46-009i5-R]	The OSI Layer Functionality of CIN-P switches shall operate at Layer 2 (Data Link Layer) of the OSI model, enabling MAC address-based switching and frame forwarding.	PBS 41 VS3-PS
[41.46-009i6-R]	The VLAN Support of CIN-P switches shall support IEEE 802.1Q VLAN tagging, capable of managing multiple VLANs and supporting inter-VLAN routing if required.	PBS 41 VS3-PS
[41.46-009i7-R]	The Redundancy and Link Aggregation of CIN-P switches shall support RSTP (Rapid Spanning Tree Protocol) – IEEE 802.1w – for fast convergence and loop prevention.	PBS 41 VS3-PS
[41.46-009i8-R]	The Redundancy and Link Aggregation of CIN-P switches shall support LACP (Link Aggregation Control Protocol) – IEEE 802.3ad – for dynamic link aggregation and redundancy.	PBS 41 VS3-PS
[41.46-009i9-R]	For the PBS 41 VS3-PS PIS cubicle connection, PBS 46 shall provide two CIN redundant SMF patch cables to the PBS 41 VS3-PS CIN Patch Panel inside the PBS 41 VS3-PS PIS cubicle. The interface point is on the PBS 41 VS3-PS CIN Patch Panel.	PBS 46
[41.46-009i10-R]	The cabling of CIN within an I&C cubicle or between I&C cubicles of PBS 41 VS3-PS shall be in the scope of PBS 41 VS3-PS.	PBS 41 VS3-PS
[41.46-009i11-R]	PBS 46 shall allocate an IP address to each of the component of PBS 41 VS3-PS PIS connected to CIN-P	PBS 46
[41.46-009i12-R]	The PBS 41 VS3-PS F-PIS cubicle shall have two media converters for redundant connection to PBS 46 CIN-P network	PBS 41 VS3-PS
[41.46-009i13-R]	PBS 41 VS3-PS F-PIS design shall respect the PBS 46 electrical characteristic for the physical interface	PBS 41 VS3-PS
[41.46-009i14-R]	PBS 41 VS3-PS shall allow CIS to manage the process to merge the different slow PIC PLC S7 projects interfacing CIS into one S7 “Multiproject”	PBS 41 VS3-PS and PBS 46

[41.46-009i15-R]	The critical automatic data between PBS 41 VS3-PS slow PIC and CIS shall be exchanged based on SIEMENS S7 fault tolerant connections with a safety message frame (F_SEND/F_RCV) between the F-CPU (communication via CIN-P)	PBS 41 VS3-PS and PBS 46
[41.46-009i16-R]	PBS 46 shall send the critical manual data from CIS Supervisor Module to PBS 41 VS3-PS slow PIS	PBS 46
[41.46-009i17-R	HIOC protocol (over Standard S7 communication) shall be implemented both in the CIS Supervisor Module and PBS 41 VS3-PS slow PIS	PBS 41 VS3-PS and PBS 46
[41.46-009i18-R]	The HIOC library delivered by PBS 46 shall be deployed/used in the PBS 41 VS3-PS slow PIC	PBS 41 VS3-PS
[41.46-009i19-R]	The critical automatic data PBS 41 VS3-PS F-PIC and PBS 46 fast controllers shall be performed using Manchester code communication over redundant optical links	PBS 41 VS3-PS and PBS 46
[41.46-009i20-R]	Each host PC of the PBS 41 VS3-PS F-PIC shall be connected to CIN patch panels via CIN-P switches using TCP/IP communication protocol	PBS 41 VS3-PS
[41.46-009i21-R]	PBS 46 shall send the critical manual data from CIS Supervisor Module to PBS 41 VS3-PS fast PIS	PBS 46
[41.46-009i22-R]	HIOC protocol shall be implemented both in the CIS Supervisor Module and PBS 41 VS3-PS fast PIS	PBS 41 VS3-PS and PBS 46
[41.46-009i23-R]	PBS 41 VS3-PS shall send PIS supervision data from PBS 41 VS3-PS slow PIS to PBS 46 Supervisor Module via standard S7 protocol	PBS 41 VS3-PS
[41.46-009i24-R]	PBS 41 VS3-PS shall send PIS archiving data from PBS 41 VS3-PS slow PIS to PBS 46 Supervisor Module via S7 TSPP protocol which enable spontaneous transmission of data and the generation of time stamps in the plant interlock controller	PBS 41 VS3-PS
[41.46-009i25-R]	The TSPP library delivered by PBS 46 shall be used in the PBS 41.V3 slow PIC	PBS 41 VS3-PS
[41.46-009i26-R]	The OPC UA server shall be provided in PBS 41 VS3-PS F-PIC host to interface with OPC UA client in CIS Supervisor Module	PBS 41 VS3-PS
[41.46-009i27-R]	In order to handle supervision data, archiving data and critical manual data between PBS 41 VS3-PS F-PIC's Host PC and CIS Supervisor Module, OPC UA communication link shall be deployed and used	PBS 41 VS3-PS and PBS 46

Table 6-1: List of Interface Requirements

7 Interface Requirement Data

7.1 Physical interface tables

Cable No.	Part Number	From Component (PPPPPP-TTT-NNNN)	From Component Description	From Location	To component (PPPPPP-TTT-NNNN)	To component Description	To Location
4601IN-CAO-nnny	FS0xF9LN	450513-CNP-0001	CNP	B13-L1-01	41V3IC-SWT-2001 41V3IC-RIO-2001 (in 41V3IC-CU-2101)	CIN Patch Panel for F-PIS	B13-L1-01
4601IN-CAO-nnnz	FS0xF9LN	450513-CNP-0001	CNP	B13-L1-01	41V3IC-SWT-2002 41V3IC-RIO-2002 (in 41V3IC-CU-2101)	CIN Patch Panel for F-PIS	B13-L1-01

Table 7-1: Patch cord list applicable to Network & P2P interfaces

Item	Functional Reference (PPPPPP-TTT-NNNN)	IP address	Subnet Mask
PIC-VS3L	41V3IC-PLC-2xxx	[To be filled]	[To be filled]
PIC-VS3U	41V3IC -PLC-2xxx	[To be filled]	[To be filled]
F-PIC Host-PC1	41V3IC -PCF-2001	[To be filled]	[To be filled]
F-PIC Host-PC2	41V3IC -PCF-2002	[To be filled]	[To be filled]
CIN-P1 switch	41V3IC -SWT-2001	[To be filled]	[To be filled]
CIN-P2 switch	41V3IC SWT-2002	[To be filled]	[To be filled]

Table 7-2: IP address allocation

7.2 Interface Data Sheet

The functional interface data are managed by Interface Data Sheet [RD6].